Notice of References Cited	Application/Control No. 09/773,853	Applicant(s)/Patent Under Reexamination SAN ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,570,842	05-2003	Landolsi, Mohamed A.	370/210
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Altera News & Views First Quarter February 2000 pg. 1-44.
	V	Hussein et al., "Design and Verification Techniques Used in a Graduate Level VHDL Course". IEEE Frontiers in Education Conference Nov.10-13 1999 pg.28-31.
	W	FIR Compiler MegaCore Function verstion 2.6.0 . 1995-2003 pg.1-5.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.